

## **In the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

## **Listing of Claims**

1. (currently amended): A high voltage device comprising:  
a substrate ~~of a first type~~;  
first and second wells respectively of ~~[[the]]~~ a first type and a second type in the substrate;  
a gate formed on a junction between the first and second wells, without a field oxide between the gate and the first and second wells;  
first and second doped regions both of the second type, respectively formed in the first and second wells and both sides of the gate;~~[[and]]~~  
a third doped region of the first type in the first well and adjacent to the first doped region~~[[.]]; and~~  
a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate.
2. (original): The high voltage device as claimed in claim 1 further comprising field oxides isolating the high voltage device from other devices on the substrate.
3. (original) The high voltage device as claimed in claim 1, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.
4. (cancelled).
5. (original): The method of claim 4, wherein third oxide layer is grown by thermal oxidation.

6. (cancelled).

7. (previously presented): The high voltage device as claimed in claim 1, wherein the first and second types are respectively P and N types.

8. (previously presented): The high voltage device as claimed in claim 1, wherein the first and second types are respectively N and P types and the high voltage device further comprises a N+ buried layer in the substrate and beneath the first and second wells.

9. (currently amended): A high voltage device formed on a P substrate comprising:  
an HVNMOS comprising:  
first P and N wells in the P substrate;  
a first gate formed on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;  
two first N+ doped regions respectively formed in the first P and N wells, and both sides of the first gate; [[and]]  
a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and  
an N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate ; and  
a HVPMOS comprising:  
an N+ buried layer in the P substrate;  
second N and P wells in the P substrate and above the N+ buried layer;  
a second gate formed on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;  
two second P+ doped regions respectively formed in the second N and P wells, and both sides of the second gate; [[and]]  
a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well[[.]]; and

a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate.

10. (original): The high voltage device as claimed in claim 9 further comprising field oxides isolating the HVPMOS and HVNMOS from other devices on the P substrate.

11. (original): The high voltage device as claimed in claim 9, wherein each of the first and second gates comprise a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

12. (cancelled).

13. (original): The high voltage device as claimed in claim 9, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

14. (cancelled).

15. (currently amended): A method for manufacturing a high voltage device, comprising the steps of:

providing a substrate ~~of a first type~~;

forming first and second wells respectively of ~~[[the]]~~ a first type and a second type in the substrate;

forming a gate on a junction between the first and second wells, without a field oxide formed between the gate and the first and second wells;

forming first and second doped regions both of the second type, respectively in the first and second wells and both sides of the gate;[[and]]

forming a third doped region of the first type in the first well and adjacent to the first doped region~~[[.]]~~; and

forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate.

16. (original): The method as claimed in claim 15 further comprising the step of:  
forming field oxides isolating the high voltage device from other devices  
on the substrate.

17. (original): The method as claimed in claim 15, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.

18. (cancelled).

19. (original): The method as claimed in claim 15, wherein there is a spacing of the second doped region to the gate.

20. (cancelled).

21. (previously presented) The method as claimed in claim 15, wherein the first and second types are respectively P and N types.

22. (previously presented): The method as claimed in claim 1, wherein the first and second types are respectively N and P types and the method further comprises the step of:  
forming an N<sup>+</sup> buried layer in the substrate and beneath the first and second well.

23. (currently amended): A method for manufacturing a high voltage device comprising the steps of:

providing a P substrate;  
forming a HVNMOS on the P substrate by:  
forming first P and N wells in the P substrate;

forming a first gate on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;

forming two first N<sup>+</sup> doped regions respectively in the first P and N wells, and both sides of the first gate; [[and]]

forming a first P<sup>+</sup> doped region in the first P well and adjacent to the first N<sup>+</sup> doped region in the first P well; and

forming a N lightly doped region adjacent to the first N<sup>+</sup> doped region in the first P well and beneath the first gate; and

forming a HVP MOS on the P substrate by:

forming an N<sup>+</sup> buried layer in the P substrate;

forming second N and P wells in the P substrate and above the N<sup>+</sup> buried layer;

forming a second gate on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;

forming two second P<sup>+</sup> doped regions respectively in the second N and P wells, and both sides of the second gate; [[and]]

forming a second N<sup>+</sup> doped region in the second N well and adjacent to the second P<sup>+</sup> doped region in the second N well[[.]]; and

forming a P lightly doped region adjacent to the second P<sup>+</sup> doped region in the second N well and beneath the second gate.

24. (original): The method as claimed in claim 23 further comprising the step of:

forming field oxides isolating the HVP MOS and HVNMOS from other devices on the P substrate.

25. (previously presented): The method as claimed in claim 23, wherein each of the first and second gates comprises a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

26. (cancelled).

27. (original): The method as claimed in claim 23, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

28. (cancelled).